Sequential Reasoning for Optimizing Compilers under Weak Memory Concurrency

Minki Cho*
Seoul National University
Korea
minki.cho@sf.snu.ac.kr

Sung-Hwan Lee*
Seoul National University
Korea
sunghwan.lee@sf.snu.ac.kr

Dongjae Lee
Seoul National University
Korea
dongjae.lee@sf.snu.ac.kr

Chung-Kil Hur
Seoul National University
Korea
gil.hur@sf.snu.ac.kr

Ori Lahav
Tel Aviv University
Israel
orilahav@tau.ac.il

Abstract

We formally show that sequential reasoning is adequate and sufficient for establishing soundness of various compiler optimizations under weakly consistent shared-memory concurrency. Concretely, we introduce a sequential model and show that behavioral refinement in that model entails contextual refinement in the Promising Semantics model, extended with non-atomic accesses for non-racy code. This is the first work to achieve such result for a full-fledged model with a variety of C11-style concurrency features. Central to our model is the lifting of the common data-race-freedom assumption, which allows us to validate irrelevant load introduction, a transformation that is commonly performed by compilers. As a proof of concept, we develop an optimizer for a toy concurrent language, and certify it (in Coq) while relying solely on the sequential model. We believe that the proposed approach provides useful means for compiler developers and validators, as well as a solid foundation for the development of certified optimizing compilers for weakly consistent shared-memory concurrency.

CCS Concepts: • Theory of computation → Concurrency; Operational semantics; • Software and its engineering → Semantics; Compilers.

Keywords: Relaxed Memory Concurrency; Operational Semantics; Compiler Optimizations

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PLDI ’22, June 13–17, 2022, San Diego, CA, USA
© 2022 Association for Computing Machinery.
ACM ISBN 978-1-4503-9265-5/22/06.
https://doi.org/10.1145/3519939.3523718

1 Introduction

Weakly consistent shared-memory semantics (a.k.a. weak, or relaxed, memory models) aim to support a wide range of source-to-source compiler optimizations. These optimizations provide indispensable means for improving performance, especially the optimizations involving memory accesses intended to be non-racy (“non-atomics” in C/C++), which are more frequent and allow more optimizations compared to synchronization accesses (“atomics” in C/C++).

The soundness of compiler optimizations is a contextual refinement property—the transformed piece of code should behave as prescribed by the semantics of its source under any context. For certain optimizations, mostly access reorderings and redundant access eliminations, soundness was established under multiple concrete weak memory models of different kinds [4, 6, 7, 14, 15, 18, 22, 32, 34, 38, 40, 41]. These results, however, require delicate and fragile arguments that depend on the full underlying complex memory model, which is often very different than standard operational semantics.1 This poses a significant challenge for compiler optimization developers, especially in the context of certified optimizing compilers, notably CompCert [23, 24], whose simulation-based approach for the soundness of each optimization pass cannot accommodate complex concurrency semantics.

In this paper, we study an alternative approach to establishing soundness of compiler optimizations under a weak memory model that is easier to use by compiler developers and is well-suited for integration within a certified compiler.

1Informal and pen-and-paper arguments often resulted in detecting miscompilation bugs due to subtle unexpected interaction between language features; see e.g., [8, Remark 7], [6, §2.2], and [5, 30].
The idea is to rely solely on sequential reasoning, and our main contribution is a novel sequential (i.e., single-threaded) semantics that can be safely used for analyzing thread-local optimizations under a full-fledged weak memory model.

The proposed approach goes hand in hand with the fact that compiler writers’ intuition for thread-local optimizations stems from inspecting sequential code, since, intuitively speaking, non-racy code behaves just like sequential code. In fact, validating optimizations that are correct in sequential programs has been one of the main goals in weak memory models design. Our results provide a formal justification of this intuition, and give grounds for development, verification, and testing of optimizations based on a sequential model.

Example 1.1. As a concrete simple example, consider an optimization pass that avoids unnecessary reads by locally applying a simplified “store-to-load forwarding” (SLF) as captured by the following pattern:

\[ x^{na} := v ; b := x^{na} \leadsto x^{na} := v ; b := v \]

where \( x \) is a shared variable, the \( na \) superscript denotes non-atomic access to memory, \( v \) is an arbitrary value, and \( b \) is a thread local register. In sequential programs this transformation is clearly sound. We aim to rely on sequential reasoning for justifying this transformation under weak memory.

While the idea of using sequential semantics to assist reasoning on concurrent programs is not new, our results provide two important advantages. First, while previous work \([9, 10, 16]\) studied a simple concurrency model based on locks or atomic blocks, the current paper is the first to realize this idea for a rich weak memory model with a wide spectrum of concurrency features, including atomic accesses of several kinds. In particular, we demonstrate that the proposed sequential semantics is sufficiently expressive to validate certain intricate optimizations of non-atomic accesses across atoms, which are performed by mainstream compilers (as we observed on armv8-a clang 11.0.1 and x86-64 GCC 11.2).

Example 1.2. Continuing Example 1.1, a more interesting SLF pass eliminates reads also across other instructions:

\[ x^{na} := v ; a : := x^{na} \leadsto x^{na} := v ; a ; b := v \]

What patterns of synchronization accesses (composed of C/C++ atomics) may be included in \( a \) (besides the fact that it should not contain writes to \( x \)) has been a source of confusion before \([5, \S2.2]\). As we show below, the model proposed in this paper allows one to analyze the soundness of this pass relying solely on a sequential model.

Second, in contrast to prior work \([9, 10, 16]\), we are not targeting a concurrency model based on the “catch-fire” mechanism, which triggers undefined behavior (UB) for data races like in C/C++11 \([2]\). The practical significance of this choice is that (irrelevant) load introduction is a sound program transformation in our model. In contrast, this transformation for non-atomics can never be generally sound in a catch-fire model, since it may introduce data races in the target program that do not exist in the source. Allowing load introduction is necessary to support optimizations based on speculation, which are commonly performed by compilers (clang, in particular), e.g., as a part of loop invariant code motion, loop unswitching, load-widening or when loading a vector while only a subset of elements is needed.\(^2\) (In fact, the “freeze” instruction recently introduced in LLVM is a tool to support branching on a possibly undefined value, which is often a result of load introduction \([21]\).)

Example 1.3. Consider an optimization pass performing loop invariant code motion (LCM) following the pattern:

\[
\begin{align*}
&\text{while } B \{ \alpha ; a := x^{na} ; \beta \} \leadsto \\
&\hspace{1cm} c := x^{na} ; \text{while } B \{ \alpha ; a := c ; \beta \}
\end{align*}
\]

In the case that the loop never executes (when \( B \) is false), a possibly racy (irrelevant) load of \( x \) is introduced. Thus, this transformation is unsound in catch-fire models. In contrast, we aim to validate such transformations, and again use sequential reasoning for their formal justification (with appropriate restrictions on \( \alpha \) and \( \beta \); see \( \S4 \)).

To demonstrate that sequential reasoning is adequate for validating soundness of optimizations under a weak memory model, we (formally) establish the adequacy of sequential reasoning for verifying optimizations w.r.t. PS2.1 \([8]\). The latter is a recent version of the “promising semantics”, a well-studied model \([18, 22, 36, 37]\) addressing the infamous “out-of-thin-air” problem that admits efficient mapping schemes to modern architectures, as well as several critical programming guarantees. Since this model does not include non-atomic accesses, we extend it with such accesses. In this extension, inspired by LLVM \([27]\), to allow load introduction, which is notoriously hard to support in a relaxed memory model \([14]\), racy non-atomic reads retrieve “undefined” values that can be later “frozen” into any non-deterministic value \([21]\) (rather than invoking UB as in C/C++11).

All in all, the contributions of this paper are:

1) We develop a sequential model, called SEQ, instrumenting a standard sequential memory with additional mechanisms to reason about program transformations under a weak memory model (\( \S4 \)). The sequential model abstracts away complicated interference of other threads, by, in particular, tracking permissions to perform non-atomic accesses on certain locations which are non-deterministically gained and dropped with acquire/release atomic accesses. We present two notions of behavioral refinement in SEQ that ensure refinement under weak memory with arbitrary concurrent context: a simple one (\( \S2 \)) that suffices for the vast majority of optimizations (including all those involving solely

\(^2\)See https://llvm.org/docs/Passes.html [Accessed Nov-21].
sequential programs that we will show to be adequate for reasoning about optimizations of concurrent programs under weak memory consistency: if a target program behaviorally refines a source program, then the source program can be replaced by the target program under any concurrent context assuming weak memory semantics (specifically, PS\textsuperscript{na}).

To understand the intuitions behind SEQ it is important to keep in mind the optimizations we aim to validate. First, since non-atomics are not meant for synchronization, all optimizations allowed in sequential code, including load introduction, should be validated on code involving solely non-atomics. The important exception here is unused store introduction, which is sound in sequential code (although existing compilers avoid this transformation, possibly due to security reasons—we would not want to expose secrets in memory), but trivially unsound in concurrent code, as an unused store of one thread may be read by others.

In contrast, we do not aim to allow optimizations on atomic accesses and fences. Understanding optimizations on synchronization code (via atomics) via sequential reasoning is unnatural, and, even if possible, it will significantly complicate our sequential model. Also, since atomic accesses are relatively rare in concurrent programs and often confined in libraries that are manually optimized by experts, the possible performance gain is rather limited. Although these optimizations were extensively studied (especially for C/C++11 \cite{11, 38}), to the best of our knowledge, existing compilers do not perform such optimizations.

Finally, we also aim to allow optimizations of non-atomics across atomics. As mentioned in the introduction, these are performed by mainstream compilers and have been a source of confusion before. We will also validate reorderings of relaxed accesses and non-atomics, as well as roach-motel reorderings (one-sided reordering of release/acquire and non-atomics) \cite{33}, which are not performed by current mainstream compilers but are naturally supported in SEQ.

**Concurrency constructs.** We assume that shared memory locations are divided into atomic locations (Loc\textsuperscript{at}) and non-atomic locations (Loc\textsuperscript{na}), and there is no mixing of atomic and non-atomic accesses to the same location.\(^3\) To simplify the presentation in the paper, we only present a fragment of the model consisting of non-atomics and release/acquire and relaxed reads and writes. Our Coq development includes more features: atomic read-modify-writes (RMWs), release sequences, fences (including sequentially consistent fences), strong relaxed accesses (which do not allow “load buffering” behaviors), and system calls. This covers all C/C++11 features as in \cite{20}, except for sequentially consistent accesses which are not supported by the promising semantics.

**Program representation in the paper.** To keep the presentation abstract, rather than introducing a concrete programming language syntax, we assume that the programming language is represented as a labeled transition system (LTS), with transitions labeled with the action that is performed. Below we use \(\sigma\) to denote the program state, which stores the rest of the program to run and the current local register file. Transitions take one of the following forms:

- \(\sigma \rightarrow \sigma':\) silent transitions that do not communicate with the memory (e.g., conditionals and local assignments).
- \(\sigma \xrightarrow{\text{choose}(v)} \sigma':\) transitions resolving a non-deterministic choice (Remark 3 in \$6\) explains why we need to expose these transitions.

\(^3\)The problem in supporting such mixing is the lower step of PS\textsuperscript{na} that modifies values of outstanding promises. We describe in \cite[Appendix E]{1}, why the lower operation is needed for validating certain compiler transformations and the challenge it creates for adequacy of sequential reasoning.
We assume that programs terminate in states of the form $S = (\sigma, P, F, M)$ where $\sigma$ is a parametric set of values. To support racy non-atomic reads, Val should contain a distinguished element, called “undefined value” and denoted by $\text{undef}$. In the refinement notions below, we allow the target program to return any value if the source returns $\text{undef}$. For this matter, a partial order $\sqsubseteq$ on Val is defined by: $v \sqsubseteq v' \Leftrightarrow v = v' \lor v' = \text{undef}$. This order is lifted to (partial) functions to Val pointwise.

**Remark 1.** We follow LLVM assuming that branching on $\text{undef}$ invokes UB. A “freeze” instruction can be used to non-deterministically choose a defined value for $\text{undef}$,\(^6\) which is captured by a $\text{choose}(v)$ transition in the LTS.

**States of SEQ.** In addition to the current program state $\sigma$, each state $S = (\sigma, P, F, M)$ of SEQ keeps track of:

- **Values.** We assume a parametric set Val of values. To support racy non-atomic reads, Val should contain a distinguished element, called “undefined value” and denoted by $\text{undef}$. In the refinement notions below, we allow the target program to return any value if the source returns $\text{undef}$. For this matter, a partial order $\sqsubseteq$ on Val is defined by: $v \sqsubseteq v' \Leftrightarrow v = v' \lor v' = \text{undef}$. This order is lifted to (partial) functions to Val pointwise.

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**Transitions of SEQ.** The transitions are given in Fig. 1. Each transition $S \xrightarrow{(e)} S'$ dictates its preconditions (which always require a corresponding program step), the way the different components of the state are updated, and possibly the label $e$ recorded in the trace when the transition is invoked. The latter is essential for the definition of refinement, which imposes conditions relating the traces (i.e., sequences of transition labels) of SEQ generated by the source program to those generated by the target program.

Concretely, **SILENT and CHOICE/RELAXED** transitions have no additional preconditions and, except for the program component, do not modify the state. The **CHOICE/RELAXED** transitions are recorded in the transition label as they need to match in traces of the source and of the target.

Non-atomics are handled differently depending on the permission set: when the program performs a non-atomic read from location $x$, it loads from the memory if $x$ is in the permission set (NA-READ); or loads $\text{undef}$ otherwise (RACY-NA-READ). In turn, when the program performs a non-atomic write to $x$, it writes to memory and adds $x$ to the set of written locations if $x$ is in the permission set (NA-WRITE), or invokes UB (by setting the program state to $\bot$) otherwise.

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\(^6\)See https://llvm.org/docs/LangRef.html#undefined-values and https://llvm.org/docs/LangRef.html#freeze-instruction [Accesses Nov-21].
(racy-na-write). Invoking UB is in accordance with the fact that we aim to invalidate (unused) store introduction. Note that the steps related to non-atomic accesses have no effect on the generated trace, allowing different sequences of non-atomic accesses between the source and the target.

Acquire and release accesses are used for synchronization in the underlying concurrency model. Although they provide more fine grained control than locks, it is helpful to understand an acquire read as a lock acquisition, and a release write as a lock release. In SEQ, these steps nondeterministically update the permission set and the memory, which, intuitively speaking, accounts for any possible interaction with the concurrent environment.

Concretely, acq-read nondeterministically (i) gains permissions for some set of locations (intuitively, these permissions are acquired from other threads), and (ii) gets new values (recorded in a partial function $V : \text{Loc}^\alpha \rightarrow \text{Val}$) for the locations in this set. Dually, rel-write nondeterministically loses permissions for some set of locations (intuitively, they are released to other threads). The rel-write transition also resets the written locations set $F$. Thus, $F$ tracks written non-atomic locations since the last release, which is needed in order to ensure that (possibly racy) writes cannot be introduced after a release, even if the location was written to (by the source) before the release (see Example 2.10).

In addition, acq-read and rel-write record in the trace (i.e., on their transition labels) the permission set before and after the transition, the written locations set, and the current memory (its updated part in acq-read and “potentially released” memory in rel-write). All these are needed for having sufficiently expressive traces that allow us to define an adequate refinement notion.

**Behavioral refinement.** We first define what constitutes a behavior in SEQ.

**Definition 2.1.** A behavior (in SEQ) is a pair of the form $⟨tr, r⟩$, where $tr$ is a finite sequence of transition labels, and $r$ is either $\text{trm}(v, F, M)$ denoting normal termination returning $v$ with written flags set $F$ and memory $M$, $\text{prt}(F)$ denoting a partial (ongoing) execution with current written flags set $F$, or $⊥$ denoting erroneous termination. We write $S \downarrow ⟨tr, r⟩$ to mean that a state $S$ generates the behavior $⟨tr, r⟩$, which is inductively defined as follows:

$$r = \begin{cases} \text{trm}(v, F, M) & \sigma = \text{return}(v) \\ \bot & \sigma = \bot \\ \text{prt}(F) & \text{otherwise} \end{cases}$$

We use standard notations for traces: $ε$ for the empty trace, $tr_1 \cdot tr_2$ for appending traces, and $α \in tr$ for occurrence of a label in a trace. We identify a label $e$ with a trace of length one when writing expressions like $e \cdot tr$.

**Example 2.2.** For a program state $σ$ that corresponds to $x^{1x} := 1; y^{tα} := 2; \text{return}(3)$, the state $S = (σ, P, θ, M)$ with $y \in P$ has the following behaviors in SEQ: $⟨ε, \text{prt}(θ)⟩$, $⟨\text{trm}(x^{1x}(1), \text{prt}(θ))⟩$, $⟨\text{trm}(x^{1x}(1), \text{prt}(t))⟩$, and the terminating behavior $⟨\text{trm}(3, [y], M[y \mapsto 2])⟩$. If $y \notin P$, then $⟨\text{trm}(x^{1x}(1), ⊥)⟩$ is the only terminating behavior. △

Next, we present the (first) notion of behavioral refinement between programs in SEQ. As standard, one may start by requiring that every behavior $⟨tr_{tgt}, r_{tgt}⟩$ of the target program is also a behavior of the source program. However, to support various optimizations, naïve inclusion does not suffice. Instead, we allow the source to generate a matching behavior $⟨tr_{src}, r_{src}⟩$ that is “less committed” than $⟨tr_{tgt}, r_{tgt}⟩$ (denoted $⟨tr_{tgt}, r_{tgt}⟩ \sqsubseteq ⟨tr_{src}, r_{src}⟩$): the source may return when the target returns a normal value ($e_{tgt} \sqsubseteq v_{src}$), end with “less defined” memory ($M_{tgt} \sqsubseteq M_{src}$), and write to more non-atomic locations ($F_{tgt} \subseteq F_{src}$). The same holds along the trace: for values recorded in atomic writes, for memories recorded in release writes, and for written locations sets recorded in acquire and release accesses. Finally, UB by the source allows any continuation by the target. All these are formally captured by the next definition:

**Definition 2.3.** The relation $\sqsubseteq$ on transition labels, traces, and behaviors is given by:

1. Transition labels:

$$e \sqsubseteq e \quad \frac{v_{tgt} \sqsubseteq v_{src}}{w^{1x}(x, v_{tgt}) \sqsubseteq w^{1x}(x, v_{src})} \quad \frac{S_{tgt} \sqsubseteq S_{src}}{F_{tgt} \sqsubseteq F_{src}}$$

2. Traces:

$$w^{ε}(x, t_{tgt}, P, P', F_{tgt}, V_{tgt}) \sqsubseteq w^{ε}(x, t_{src}, P, P', F_{src}, V_{src})$$

3. Behaviors:

$$\langle tr_{tgt}, M_{tgt}, M_{src} \rangle \sqsubseteq \langle tr_{src}, F_{src}, F_{tgt}, V_{src} \rangle$$

**Definition 2.4.** We write $S_{src} \sqsubseteq S_{tgt}$ if $S_{src} \downarrow ⟨tr_{src}, r_{src}⟩$ implies that $S_{src} \downarrow ⟨tr_{src}, r_{src}⟩$ for some behavior $⟨tr_{src}, r_{src}⟩$ such that $⟨tr_{tgt}, r_{tgt}⟩ \sqsubseteq ⟨tr_{src}, r_{src}⟩$. A program state $σ_{tgt}$ behaviorally refines a program state $σ_{src}$, denoted by $σ_{tgt} \sqsubseteq σ_{src}$, if $σ_{tgt} \sqsubseteq σ_{src}$, if $⟨σ_{tgt}, P, F, M⟩ \sqsubseteq ⟨σ_{src}, P, F, M⟩$ for every $P, F, M$.

Next, we present a sequence of examples demonstrating several subtleties in the above definitions. In these examples, when writing $prog_{src} \leadsto prog_{tgt}$ for two code snippets $prog_{src}$ and $prog_{tgt}$, we mean that for any (sequential) context $C$, the state $σ_{tgt}$ that corresponds to $C(prog_{tgt})$ (with some
initial register file) behaviorally refines the state $\sigma_{src}$ that runs $C[prog_{src}]$ (with the same initial register file). We write $\neg prog_{src} \Rightarrow prog_{tgt}$ for the negation of $prog_{src} \leadsto prog_{tgt}$.

**Remark 2.** Our results that are formalized in Coq also address reasoning about program transformations in SEQ. In particular, they allow one to lift local refinement properties (such as the ones listed in the examples below) to any sequential context $C$. Concretely, we define a simulation relation between SEQ states and prove that it admits certain congruence properties. Then, by establishing simulation between $prog_{src}$ and $prog_{tgt}$, we can derive $\neg prog_{src} \Rightarrow prog_{tgt}$ as defined above. Since these techniques are fairly standard in compiler verification, and our main focus is to reduce reasoning about concurrent code to reasoning about sequential code, we omit these details from the paper. In the example below, we intend to give the right intuitions, rather than precise refinement arguments.

**Example 2.5 (Reordering of non-atomics).** Non-atomic accesses to different locations can be freely reordered in SEQ, e.g., $a := x^n; y^n := \mathcal{V} \leadsto y^n := \mathcal{V}; a := x^n$ where $x \neq y$. Consider a general context $C$, and let $\sigma_{src}$ and $\sigma_{tgt}$ be the program states that correspond to $C[a := x^n]; y^n := \mathcal{V}$ and $C[y^n := \mathcal{V}; a := x^n]$, respectively, with the same initial register file. Suppose that $(\sigma_{tgt}, F, P, M) \not\parallel (\sigma_{src}, F, P, M)$. Then, by executing two steps in the source (a read from $x$ followed by a write to $y$) at the time the target executes its write to $y$, one can show that $(\sigma_{src}, F, P, M) \not\parallel (\sigma_{tgt}, F, P, M)$. In particular, after the target performs the read, the source and the target reach the same program state.

On the other hand, reordering of non-atomics to the same location is disallowed, e.g., the reordering of a load followed by a store $a := x^n; x^n := 1 \Rightarrow x^n := 1; a := x^n$. Indeed, for the context $C = \cdot : return(a)$, we have $\sigma_{tgt} \not\parallel (\sigma_{src}, F, P, M)$. If the target invokes UB and generates $(\epsilon, \bot)$, then it must be the case that we started without permission on $x$, and the source may invoke UB and generate $(\epsilon, \bot)$ as well. Thus, in order to obtain a behavior of the target that is not matched by a behavior of the source, in the case the loop is non-terminating, we must consider behaviors before termination $(\epsilon, pr\mathcal{T}(F))$. Indeed, when starting with permission on $x$ and $M(x) = 1$, the target generates $(\epsilon, pr\mathcal{T}(\{x\}))$, but, if the loop does not terminate, the only behavior of the source is $(\epsilon, \emptyset)$.

In contrast, reads may be reordered with possibly non-terminating local computation:

$$\text{while} \ldots \text{do} \ldots ; a := x^n \leadsto a := x^n; \text{while} \ldots \text{do} \ldots$$

Indeed, in partial traces only the written locations set $F$ has to match, and this set is the same in executions of the two programs.

**Example 2.8 (Unused load elimination and introduction).** The transformations that eliminate/introduce an unused load $a := x^n \leadsto \text{skip} \leadsto a := x^n$ trivially correspond to behavioral refinements in SEQ. For the latter, we need that a non-atomic read without permission does not invoke UB. We note that in the paper presentation, we have to assume that $a$ does not occur in the context. Nevertheless, our Coq formalization that uses interaction trees can easily express a computation that reads a value and does not return the result to its continuation. This computation is interchangeable with a no-op under any context.
Example 2.9 (Reordering of atomics and non-atomics). Reordering of atomic and non-atomic accesses follows the “roach-motel” principle. The following are forbidden:

(i) \( a := x^{acq}; y^{na} := v \leadsto y^{na} := v; a := x^{acq} \)

(ii) \( y^{na} := v; x^{rel} := v \leadsto x^{rel} := v; y^{na} := v' \)

(iii) \( a := x^{acq}; b := y^{na} \leadsto b := y^{na}; a := x^{acq} \)

(iv) \( a := y^{na}; x^{rel} := v \leadsto x^{rel} := v; a := y^{na} \)

In (i), starting without permission on \( y \) (\( y \notin P \)), the target invokes UB, thus generating the behavior \( (\epsilon, \perp) \). The source, however, has to perform the acquire read before invoking UB, thus generating terminating behaviors of the form \( (R^{acq}_x, \perp) \) only.

In (ii), if the release write to \( x \) loses the permission on \( y \) (transitioning from a state with \( y \in P \) to a state with \( y \notin P \)), then the target program invokes UB, generating a behavior of the form \( (\perp, \perp) \). However, since we start with \( y \in P \), the source does not invoke UB, and cannot generate any behavior of the form \( (\perp, \perp) \).

In (iii), for the context \( C = ; return(b) \), if a permission on \( y \) is gained by the acquire read from \( x \), and we start with \( y \notin P \) (and \( M(y) \neq \text{undef} \)), the target generates a behavior of the form \( (R^{acq}(x,\perp, P \cup \{y\}, \perp), \text{trm}(\text{undef}_y, \perp)) \), whereas the source cannot perform racy read on \( y \).

In (iv), for the context \( C = ; return(a) \), if we start with \( y \in P \), and this permission is lost by the release write, the target generates a behavior of the form \( (\perp, \text{trm}((\text{undef}_y, \perp)), \perp) \), whereas the source cannot perform racy read on \( y \) at all.

Next, the following converses of the above are validated:

(i') \( y^{na} := v; a := x^{acq} \leadsto a := x^{acq}; y^{na} := v \)

(ii') \( b := y^{na}; a := x^{acq} \leadsto a := x^{acq}; b := y^{na} \)

(iii') \( x^{rel} := v; a := y^{na} \leadsto a := y^{na}; x^{rel} := v \)

For (i') we use the fact that acquire transitions of the target can be matched by acquire transitions of the source annotated with \( F_{rel} \subseteq F_{acq} \) (since we may have \( y \in F_{rel} \) but not \( y \in F_{acq} \) when performing the acquire), as well as the fact that the source may invoke UB earlier than the target (in particular, \( (R^{acq}_x, \perp) \subseteq (\epsilon, \perp) \)). In turn, (iii') and (iv') demonstrate the need in allowing the source to return \( \text{undef} \) when the target returns a defined value. This is needed, for instance, if the acquire read in (iii') gains permission on \( y \).

Finally, despite being a valid roach-motel reordering, the converse of (ii) is disallowed by the current behavior refinement. It is supported by the more refined notion in §3.

Example 2.10. Stores cannot be introduced even if they already occur before a release write:

\( x^{na} := v; y^{rel} := 1 \leadsto x^{na} := v; y^{rel} := 1; x^{na} := v \)

Intuitively, if a write is protected by a lock, another one should not be introduced after the lock is released. Formally, since release writes reset the written locations set, the target’s terminating behavior has \( x \in F \), while the source ends with \( F = \emptyset \). In contrast, the transformation is validated with \( r^{lx} \) instead of \( r^{rel} \) above.

Example 2.11 (Store-to-load forwarding across atomics). Reads can be eliminated after writes across atomics:

\( x^{na} := v; a := x^{acq}; b := x^{na} \leadsto x^{na} := v; a := x^{acq}, y^{rel} := v' \).

where \( a \in \{a := y^{ril}, y^{ril} := v', a := y^{acq}, y^{rel} := v'\} \).

If we start with \( x \notin P \), the source raises UB, and generates \( (\epsilon, \perp) \), which matches any target behavior. Otherwise, the relevant write step of the source set \( M(x) = v \), and \( M(x) \) is not altered by \( a \) (in particular, it is important here that an acquire read can only modify values of locations that gained permission). Thus, either \( v \) is read by \( b := x^{na} \), or, if \( a \) corresponds to a release write that transferred the permission on \( x \), the source will read \( \text{undef} \), and we have \( v \subseteq \text{undef} \). In any case, the source matches every behavior of the target.

Example 2.12. Reads cannot be eliminated after writes across release-acquire pairs:

\( x^{na} := v; y^{acq} := v' \leadsto a := y^{acq}; b := x^{na} \leadsto x^{na} := v; y^{rel} := v'; a := y^{acq}; b := v \)

Intuitively, another thread may safely access \( x \) between the release and the acquire and change its value. To see this in SEQ, consider the execution of the target program when permission to \( x \) is lost by the release write, and regained by the acquire read. The updated portion of the memory \( V \), including a new (non-deterministic) value for \( x \), is recorded on the acquire transition in the trace. To match the behavior of the target, the source program has to have the same updated memory in its acquire transition, and when \( V(x) \neq v \), the source will not be able to later read \( v \) from \( x \). This example demonstrates the need in updating the values in memory (for locations that gained permission) in acquire steps.

3 Advanced Behavior Refinement

As we show in §6, the above notion of behavioral refinement in SEQ is adequate for reasoning about optimizations in the promising semantics. As shown above, it is also precise enough to verify a variety of optimizations. However, optimizations including both an atomic access and a non-atomic write are beyond its power: although they are meant to be sound (and they are sound in the promising semantics), the above notion invalidates them. In this section, we discuss this issue that stems from two different reasons, and then present a more refined notion of behavioral refinement (implied by the simple one above) that addresses this challenge. We note that, since our result in §6 provides contextual refinement, one may mix and match—prove most optimization passes using the simple notion in §2, and use the one of this section for several more involved program transformations.

Late UB. A simple example of a sound optimization that is invalidated by the above notion is the following:

\( a := x^{ril}; y^{na} := v \leadsto y^{na} := v; a := x^{ril} \)
Indeed, the reasoning in Example 2.9 (i) that shows why an acquire read followed by a non-atomic write cannot be reordered applies as is in this case as well: starting without permission on \( y \neq P \), the target program invokes UB, thus generating the behavior \( (\epsilon, \bot) \).

The source, however, has to perform the relaxed read before invoking UB, thus generating terminating behaviors \( (tr_{src}, \bot) \) with \( tr_{src} \) consisting of a \( R^{1x} \) label. Intuitively, however, this should not matter since the source program anyway invokes UB, in which case the target's behavior is immaterial. Thus, we would like to allow to match any behavior \( (tr_{tgt}, r_{tgt}) \) of the target program by any UB behavior \( (tr_{src}, L) \) of the source. Nevertheless, for two reasons, this solution requires extra care.

First, it essentially allows reordering of any access with an operation that invokes UB, e.g., \( \alpha ; a := \alpha/0 \leadsto a := \alpha/0 ; \alpha \).

As the next example shows, in concurrent settings this reordering must be invalidated if \( \alpha \) contains an acquire read.

**Example 3.1.** Consider the following optimizations:

\[
\begin{align*}
    a & := x^{r1x} ; \quad a := x^{r1x} ; \quad y^{r1x} := 1 ; \\
    \text{if} \ a = 1 & \text{then} \quad \text{if} \ a = 1 \text{then} \quad a := x^{r1x} ; \\
    a & := x^{acq} ; \quad b := 1/0; \quad \text{leadsto} \quad a := x^{r1x} ; \\
    b & := 1/0 \quad a := x^{acq} \quad b := 1/0; \\
    \text{else} \ y^{r1x} := 1 & \text{else} \ y^{r1x} := 1 \quad a := x^{acq}
\end{align*}
\]

First, we perform the (unsound) reordering of an acquire read with UB-invoking operation. Then, a sequence of standard optimizations (start with \( b := 1/0 \leadsto y^{r1x} := 1 ; b := 1/0 \), then hoist \( y^{r1x} := 1 \) from both branches of the conditional and reorder it with \( a := x^{r1x} \)) leads to the program on the right. Now, if the concurrent context consists of another thread with the code: \( c := y^{r1x} ; x^{rel} := c \), then UB is possible for the target, but not for the source.

Thus, to keep invalidating the reordering of an acquire operation followed by UB, we require that there are not any acquire accesses in the suffix of the source trace \( tr_{src} \) (in the source’s path towards UB) that does not match the target’s trace \( tr_{tgt} \). For instance, this invalidates the transformations \( a := x^{acq} ; b := 1/0 \leadsto b := 1/0 ; a := x^{acq} \) and \( a := x^{acq} \). \( y^{na} := v \leadsto y^{na} := v ; a := x^{acq} \) if we start without permission on \( y \), the target’s behavior \( (\epsilon, \bot) \) does not match any source behavior.

Second, it is crucial to make sure that for executing this suffix, the source does not make assumptions on the environment. To see this, consider the following example:

\[
\begin{align*}
    a & := x^{r1x} ; \quad a := x^{r1x} ; \quad b := 1/0; \quad a := x^{r1x} ; \\
    \text{while} \ldots & \text{do} \ldots \quad \text{leadsto} \quad \text{while} \ldots \text{do} \ldots \quad \text{do} \ldots
\end{align*}
\]

Without additional restrictions, since we allow any behavior of the target to be matched with \( \langle R^{1x}(x), 1 \rangle \) of the source, this transformation, which is clearly unsound (even in sequential programs), will be validated by SEQ. Intuitively speaking, what went wrong here is that the source matches the UB of the target by reading 1 from \( x \), whereas a concurrent environment may not provide this option.

To address this issue, when we match the UB of the target by a suffix of source trace that leads to UB we need to make sure that the source avoids making assumptions on the concurrent environment. Technically, we achieve this by assuming that read values of atomic reads, permission gains and losses, and memory updates (\( V \) on acquire transitions) are dictated by an oracle, which intuitively represents a possible concurrent environment. We then require that behavioral refinement holds for any oracle (which has to satisfy certain progress and monotonicity conditions that any environment satisfies). In particular, in the example above, the source has to match the target’s UB also for an oracle that forces the source to read \( x \neq 1 \), in which case the source cannot invoke UB. In contrast, in the earlier example for the need in late UB \( (a := x^{r1x} ; y^{na} := v \leadsto y^{na} := v ; a := x^{r1x}) \), if we start without permission on \( y \), the source invokes UB for any oracle as its write is independent of an acquire read.

**Writes across release.** Roach motel reordering of a release write followed by a non-atomic write pose another challenge to sequential reasoning:

\[
\begin{align*}
    x^{rel} := v & ; y^{na} := v' \leadsto y^{na} := v' ; x^{rel} := v
\end{align*}
\]

Even if we modify behavioral refinement as discussed above, some behaviors of the target are not matched by the source. Concretely, starting with permission on \( y \), the target’s label \( w^{rel}(x, u, P, P', F_{tgt}, V_{tgt}) \) must have \( y \in F_{tgt} \) and \( V_{tgt}(y) = v' \), whereas the source is confined by the initial state (which may have \( y \notin F_{src} \) or \( V_{src}(y) \neq v' \)). Intuitively, this should not be a problem: the source is going to write to \( y \) after the release, and other threads can observe that write.

To solve this, we need to allow the source to generate release labels with different written locations set and memory compared to the target’s labels, provided that later on the source will write to the non-atomic locations that were different. Technically, we achieve this by parameterizing behavioral refinement with a “commitment set” \( R \), which is a set of non-atomic locations that the source program must write to before it terminates or executes an acquire read. (Fulfilling commitments after an acquire read corresponds to the disallowed reordering of writes after an acquire read.) Initially, the commitment set is empty. Then, we modify (remove fulfilled commitments and add new ones) this set with every release transition. In the end of the execution and with every acquire transition, we verify that all commitments were fulfilled. Finally, the non-terminating behaviors \( \langle tr, prt(F) \rangle \) should allow the source program to continue its execution and fulfill the outstanding commitments.

**Advanced behavior refinement.** The above solutions are formalized as follows. First, when checking for refinement between a source program and a target program in SEQ, we use an oracle to represent the environment of the thread. To pass only relevant information to the oracle, we use the following notion for stripping transition labels
Sequential Reasoning for Optimizing Compilers under Weak Memory Concurrency
PLDI ’22, June 13–17, 2022, San Diego, CA, USA

With the above definition, the more refined behavioral refinement notion is stated as follows:

**Definition 3.3.** A program state \( \sigma_{\text{tgt}} \) weakly behaviorally refines a program state \( \sigma_{\text{src}} \), denoted by \( \sigma_{\text{tgt}} \sqsubseteq_w \sigma_{\text{src}} \), if for every oracle \( A \), if \( \langle \sigma_{\text{tgt}}, P, F, M \rangle \not\sqsubseteq \langle \sigma_{\text{src}}, P, F, M \rangle \) and \( \tau_{\text{tgt}} \in \text{Tr}(A) \), then \( \langle \sigma_{\text{src}}, P, F, M \rangle \not\sqsubseteq \langle \tau_{\text{src}}, r_{\text{src}} \rangle \) for some \( \langle \tau_{\text{src}}, r_{\text{src}} \rangle \) such that \( \langle \tau_{\text{tgt}}, r_{\text{tgt}} \rangle \sqsubseteq_r \langle \tau_{\text{src}}, r_{\text{src}} \rangle \) and \( \tau_{\text{src}} \in \text{Tr}(A) \).

**Proposition 3.4.** \( \sigma_{\text{tgt}} \sqsubseteq \sigma_{\text{src}} \Rightarrow \sigma_{\text{tgt}} \sqsubseteq_w \sigma_{\text{src}} \).

**Example 3.5** (Overwritten store elimination across atoms). Consider the elimination of a write after another write to the same location across an atomic access:

\[ x^{\text{na}} := v ; \alpha ; x^{\text{na}} := v' \sim \alpha ; x^{\text{na}} := v' \]

where \( \alpha \in \{ b := y^{1L}, y^{1L} := v_y, b := y^{\text{ac}}, y^{\text{el}} := v_y \} \). The three cases except for \( \alpha = y^{\text{el}} := v_y \) are easily validated by the simple behavioral refinement in SEQ (here it is needed that the source may have larger \( F \) sets).

The case that \( \alpha \) is a release write should be also considered sound, since, roughly speaking, other threads that can observe \( x^{\text{na}} := v \) can always also observe \( x^{\text{na}} := v' \) instead. (In particular, this optimization is sound in the promising semantics.) Nevertheless, the simple refinement notion in §2 invalidates this optimization (\( \sigma_{\text{tgt}} \not\sqsubseteq \sigma_{\text{src}} \)): starting with permission on \( x \), the memory recorded in release writes in the source is confined to have \( M(x) = v \), while the target has the value of the initial memory. In turn, we do have \( \sigma_{\text{tgt}} \sqsubseteq_w \sigma_{\text{src}} \). In particular, consider the empty context, and let \( \text{rel}(P, F, u) := y^{\text{rel}}(y, v_y, P, P', F, M[x \mapsto u]) \). If we start with permission on \( x \) and do not release it, then for \( r = \text{trm}(\text{unit}, \{ x \}, M[x \mapsto v']) \),

\[ \langle \text{rel}(\{ x \}, \{ x \}, v, r) \rangle \sqsubseteq \langle \text{rel}(\{ x \}, \{ x \}, \emptyset, M(x)) \rangle \]

follows from \( \langle e, r \rangle \sqsubseteq (x, r) \). If we start with permission on \( x \) and release it, then

\[ \langle \text{rel}(\{ x \}, \emptyset, \{ x \}, v, \bot) \rangle \sqsubseteq \langle \text{rel}(\{ x \}, \emptyset, \emptyset, M(x)) \rangle \]

follows from \( \langle e, \bot \rangle \sqsubseteq (x, \bot) \). If we start without permission on \( x \), then, using BEH-FAILURE, we have:

\[ \langle \text{rel}(\emptyset, \emptyset, \{ x \}, v, \bot) \rangle \sqsubseteq (e, \bot) \].

---

\(^6\)Currently, it is not performed by mainstream compilers (checked for armv8-a clang 11.0.1 and x86-64 GCC 11.2).
4 A Certified Optimizer

We implemented in Coq a verified optimizer that optimizes an arbitrary program written in WHILE, a simple C-like language, that is interpreted as an interaction trees program, for which our adequacy theorem in §6 is stated. The optimizer’s correctness proof relies solely on SEQ, thus showcasing the applicability of SEQ for compiler verification.7

The optimizer statically analyzes a given sequential program by performing a fixpoint computation in an abstract semantics and optimizes the program based on the static analysis. Generally speaking, the analysis result assigns predicates on states of SEQ to each program point. Using the analysis result, the optimizer transforms the program, for instance, a non-atomic read from x into a register assignment if the analysis ensures that x has certain value.

The optimization process consists of four optimization passes, store-to-load forwarding (SLF), load-to-load forwarding (LLF), dead (overwritten) store elimination (DSE), and loop invariant code motion (LICM), which, on the memory trace level, are captured as follows:

\[
\begin{align*}
\text{SLF} & : x^{na} := v; \alpha; b := x^{na} \rightarrow x^{na} := v; \alpha; b := v \\
\text{LLF} & : a := x^{na}; \beta; b := x^{na} \rightarrow a := x^{na}; \beta; b := a \\
\text{DSE} & : x^{na} := a; \gamma; x^{na} := b \rightarrow \text{skip}; \gamma; x^{na} := b \\
\text{LICM} & : \text{while} (\ldots) \rightarrow \{ \beta_1 : a := x^{na}; \beta_2 \} \rightarrow c := x^{na}; \text{while} (\ldots) \rightarrow \{ \beta_1 : a := c; \beta_2 \}
\end{align*}
\]

where \(\alpha\) contains no writes to \(x\) or release-acquire pairs, \(\beta, \beta_1, \beta_2\) contain no writes to \(x\) or acquire reads, and \(\gamma\) contains no reads from \(x\) or release-acquire pairs.

Next, we focus on the SLF pass and describe the analysis and optimization in detail. The other passes are described in [1, Appendix D]. Figure 3 depicts the analysis performed in the SLF pass, which forwards values written by stores to later loads, possibly across atomic operations, but not across a release-acquire pair. At every program point, the analysis assigns two kinds of information to each shared variable: a memory value to forward and a flag for detecting a release-acquire pair after the most recent write. This information is represented by the following abstract tokens:

- \(x \mapsto 0(v)\) indicates that \(v\) was written to \(x\) by the most recent write to \(x\) and a release operation has been executed while a release-acquire pair has not; and
- \(x \mapsto \top\) indicates any other case, in particular, the case when a release-acquire pair has been executed since the last write to \(x\).

The analysis starts with the initial abstract state assigning \(\top\) to every location in the initial program point. Then, it updates line-by-line the abstract state following the transition function \(T\), which gets the current instruction and the token to a location \(x\) and returns the next abstract token to \(x\). Roughly speaking, following the transformers in Fig. 3, the abstract state of \(x\) transitions to \(0(v)\) for a non-atomic write \(x^{na} := v; 0(v)\) transitions to \(\bullet(v)\) for a release write; and \(\bullet(v)\) transitions to \(\top\) for an acquire read. To show termination, we have proved that the analysis reaches a fixpoint in at most three iterations when analyzing a loop.

Given the analysis result at each program point, SLF transforms a read \(a := x^{na}\) into a register assignment \(a := v\) if the token to \(x\) is \(\bullet(v)\) or \(0(v)\) at that program point. Intuitively, having \(x \mapsto \bullet(v)\) or \(x \mapsto 0(v)\) means that no release-acquire pair has been executed since \(v\) was written to \(x\), thus the memory value of \(x\) is still \(v\) even if the thread has lost the permission to \(x\). The transformation is sound since the thread will read \(v\) or \(\text{undef}\) from \(x\) depending on whether the permission to \(x\) has been lost or not. Formally, a reachable SEQ state \((\sigma, P, F, M)\) is related to the analysis result at the relevant program point as follows:

\[
\forall x. \begin{cases} 
  x \in P \land v \subseteq M(x) \quad & \text{if } x \mapsto 0(v) \\
  x \in P \land v \subseteq M(x) \quad & \text{if } x \mapsto \bullet(v)
\end{cases}
\]

Figure 4 describes how the analysis and optimization work for a concrete program example.

The verification of the passes is executed by (i) establish the soundness of each analysis; and (ii) from the soundness, derive a simulation in SEQ between the source and target codes. The simulation relation in SEQ (given in [1, Appendix A]) ensures advanced behavioral refinement as defined in §3.5 This verification strategy follows the standard approach of CompCert, and, importantly, the optimizer is fully verified in Coq relying solely on sequential reasoning.

5 Non-atomics in the Promising Semantics

We present the extension of PS2.1 with non-atomic accesses, which we denote by PS\(^{na}\). At the core of this extension is an operational race detection, so UB is invoked on write-write races and \(\text{undef}\) is read on read-write races. Unlike in SEQ (§2), we allow the mixing of atomic and non-atomic accesses to the same location (so we assume one set Loc of locations), which means that a race may involve only one non-atomic

---

7 In fact, it was carried out by a student with minimal understanding of weak memory consistency!
Two loads from \( x \) are optimized to register assignments. To illustrate the analysis, the code is annotated with abstract tokens to \( x \). The first instruction \( x^{na} := 42 \) induces UB if there is no permission on \( x \). Therefore, the permission on \( x \) is guaranteed, with the memory value 42 at \( x \) (which is represented by \( x \mapsto 42 \)). Since \( x \) is already permissioned, its value is not updated by the \( l := y^{rel} \), thereby maintaining the abstract state of \( x \). Upon a conditional, we keep analyzing each branch separately, and then join the results. On the \( \text{then} \) branch, \( a := x^{na} \) will load 42 from the memory as the abstract state indicates. For the next instruction, \( y^{rel} := 1 \), the abstract state of \( x \) transitions to \( x \mapsto 42 \) as the permission on \( x \) can be dropped by the release write, while the memory value at \( x \) is maintained. Finally, the branch is merged and the analysis results are joined (following the partial order on the abstract tokens). The effect of the last instruction, \( b := x^{na} \), depends on the permission on \( x \). If there is no permission on \( x \), \( y \) is read, which can be replaced by 42 by definition. In turn, the abstract state of \( x \) tells us 42 must be loaded if there is a permission on \( x \). From the above analysis, we conclude that the two loads can be replaced with register assignments.

**Figure 4. An example optimization by SLF including the underlying analysis in SEQ**

Racy accesses are naturally defined: a non-atomic access to \( x \) is racy if the thread is unaware of some message with location \( x (V(x) < m, t) \), and an atomic access to \( x \) is racy if the thread is unaware of some non-atomic message with location \( x \). Using \( \text{race-helper} \), a thread reads \( \text{undef} \) when performing a racy read (racy-read), and invokes UB on a racy write (racy-write).

For supporting the compiler transformation that replaces an \( \text{undef} \) by a non-\( \text{undef} \) value, we note that the promise lowering step in \( \text{PS}^{na} \) (lower), which allows threads to modify their own promises, also allows to change a non-\( \text{undef} \) value of a promise to \( \text{undef} \) (see [1, Appendix E]).

**Machine steps.** A machine state, which consists of the different thread states (\( T \)) and a main memory (\( M \)), can take a step by one of the threads taking a sequence of steps (machine: normal), possibly invoking UB (machine: failure). Normal steps (machine: normal) require certification: the thread that passes control to the scheduler has to show that by running alone it can fulfill all its promises.

**Example 5.1.** The following demonstrates how promises and the racy read step work:

\[
\begin{align*}
a & := x^{na} ; \quad \# \text{undef} \\
y^{rel} & := 1 \\
b & := y^{rel} ; \\
\text{if } b = 1 \text{ then } x^{na} & := 1
\end{align*}
\]

Here, the left thread may promise \( y = 1 \), since by running alone, it is able to execute the read from \( x \) and fulfill its promise. Then, the right thread reads 1 from \( y \) and writes 1 to \( x \). (Other messages may be also added to \( x \) before the \( x = 1 \) message.) Now, the non-atomic read from \( x \) of the left thread is racy since there is a message of \( x \) with timestamp larger than the thread’s view of \( x \). Thus, the thread reads \( \text{undef} \) from \( x \) and fulfills the promise \( y = 1 \).

**Results.** We ported to \( \text{PS}^{na} \) the soundness proofs of all thread-local transformations and data-race-freedom guarantees for \( \text{PS}^{2.1} \). In addition, we proved that strengthening non-atomic accesses to atomic accesses is sound. Since relaxed accesses and non-atomic are both compiled to plain machine accesses, the soundness of mapping schemes to...
We write
\[
∀ \sigma. \ V ∈ \text{View} \ (P_{\text{seq}} \models \sigma \ 0) \quad \Rightarrow \quad \text{…}
\]

### Behavioral refinement

A behavior and behavioral refinement in PS\textsuperscript{na} are defined as follows.\[^{10}\]

**Definition 5.2.** A behavior (in PS\textsuperscript{na}) is a mapping \( r : \text{Tid} \rightarrow \text{Val} \) assigning a return value to each thread or \( r = ⊥ \) for erroneous termination. We inductively define when a machine \((T, M)\) generates a behavior \( r \), denoted by \((T, M) \models r\):

\[
\forall \pi \in \text{Tid}. \quad (T(\pi), M) \models r \quad \Rightarrow \quad \langle (T(\pi), M) \rightarrow (T’, M’) \rangle \models r
\]

We write \( r_{\text{tgt}} \subseteq r_{\text{src}} \) if either \( r_{\text{src}} = ⊥ \) or \( \forall \pi. \ r_{\text{tgt}}(\pi) \subseteq r_{\text{src}}(\pi) \).

**Definition 5.3.** A concurrent program state \( ∣σ_{\text{tgt}}⟩ \) behavesally refines a concurrent program state \( ∣σ_{\text{src}}⟩ \), denoted by \( ∣σ_{\text{tgt}}⟩ \models ∣σ_{\text{src}}⟩ \), if whenever we have \( ∣\lambda. \ T(\pi), M₀⟩ \) and \( r_{\text{tgt}} \subseteq r_{\text{src}} \) (i.e., \( r_{\text{src}}(\pi) \subseteq r_{\text{tgt}}(\pi) \)), there exists \( r_{\text{src}} \) such that \( r_{\text{src}} \subseteq r_{\text{tgt}} \) and \( ∣\lambda. \ T(\pi), M₀⟩ \models r_{\text{src}} \). (Here, \( M₀ \) is the initial memory consisting of an initialization message \( x\text{null} \) for every \( x \) in \( \text{Loc} \).)

**Minit** is the initial memory consisting of an initialization message \( x\text{null} \) for every \( x \) in \( \text{Loc} \).
First, there is a large gap between SEQ’s simple states and the complex states of PS\textsuperscript{na}. Second, in PS\textsuperscript{na}, we should consider interference by other threads at every point, whereas in SEQ, memory states are changed only in release/acquire steps. Third, we need to show how promise steps of the target in PS\textsuperscript{na} are simulated by the source and establish a PS\textsuperscript{na} certification execution for every step of the source.

The key idea for the first point is that even though PS\textsuperscript{na} has complex states, not all its complexity affects non-atomic steps. In fact, a memory in SEQ can be seen as an approximation of a state in PS\textsuperscript{na} capturing only the part related to non-atomic steps. The value of a location \( x \) in SEQ corresponds to the value of the message pointed by the thread view on \( x \) in PS\textsuperscript{na}, and a permission on \( x \) in SEQ means that there is no racy message with the thread in PS\textsuperscript{na}. Since non-atomic and relaxed accesses do not change the thread view on other locations, states in SEQ are not changed after non-atomic and relaxed accesses. In turn, an acquire read in PS\textsuperscript{na} may increase the thread view, which corresponds to the modified values and gained permissions in acquire steps of SEQ.

For the second point, we need a novel insight on the promising semantics: in a machine step, it suffices to have promise steps followed by non-promise steps ending with a release write (or thread termination). This implies that racy messages of other threads are added only when a release write is executed, which corresponds to SEQ losing permissions only on a release write.

For the third point, we construct the certification steps of the source execution from those of the target. The challenge here is the two cases where the target thread fulfills its promise while the source cannot: (i) when there is no source step performing a write step of the target fulfilling a promise; and (ii) when the written message by the source has a different value than the target’s. This challenge is addressed by the commitment set of the advanced refinement, which ensures that, in both cases, the source thread should be able to write to the problematic locations in the future, thereby allowing the source to establish its certification.

Remark 3. Theorem 6.2 does not hold without the determinism premise (see [1, Appendix C] for an example). This stems from a drawback of the promising semantics (rather than due to SEQ) that we encountered while developing SEQ. Concretely, the promising semantics disallows reordering of an internal non-deterministic choice followed by a release write. By exposing non-deterministic choices (via \texttt{choose(\_)} labels), we invalidate these reorderings in SEQ and obtain adequacy for deterministic programs. (Nevertheless, the reordering of non-deterministic choices and non-atomic accesses is fully allowed by SEQ.) We leave to future work to improve the promising semantics to allow this reordering, which will allow one to remove the \texttt{choose(\_)} labels from SEQ.

7 Conclusion and Related Work

We developed a sequential model, SEQ, for reasoning about compiler optimizations in a rich weak memory model (concretely, PS\textsuperscript{na}, an extension of PS2.1 with non-atomic accesses), and demonstrated its applicability for compiler verification. This provides the first formal result establishing the adequacy of sequential reasoning for a full-fledged weak memory model without relying on catch-fire semantics for races, accompanied by the first non-trivial certified optimization algorithms for weak memory concurrency. While the ideas and intuitions behind the sequential reasoning are general, adequacy is specifically proved for PS\textsuperscript{na}. Nevertheless, we believe that SEQ can be adapted for reasoning about optimizations in other weak memory models.

Having a sequential model for compiler optimizations paves the way for future work, which has seemed to be out of reach when dealing with complicated concurrency models. This includes the extension of CompCert to weak memory concurrency (in fact, our sequential model is not far from compilers’ model of C, and the simple refinement in §2 may well suffice), as well as of automatic tools like Alive2 [28] for SMT-based translation validation.

Our results have two main limitations. First, SEQ requires the memory layouts of the source and target to be identical, which rules out certain compiler transformations that are performed by CompCert and its extensions mentioned below (although register promotion is supported by PS\textsuperscript{na}). To the best of our knowledge, these are the only thread-local optimizations on non-atomics that compilers actually perform that are unsound under SEQ. Second, our refinement notion is not termination preserving (which requires fairness assumptions, possibly following [19]). Addressing these issues is left to future work.

Next, we discuss the relation to previous work.

Sequential reasoning. The closest to our work is the work by Cuellar et al. [10] (see also [3, 9]) who develop a concurrency semantics, called “concurrent permission machine” (CPM), for CompCert that allows sequential reasoning on program optimizations. Their model has catch-fire semantics, using locks to avoid races. They also present a version of concurrent separation logic that can be used to show that a given program is race-free. While our use of permissions is inspired by these works, our results go beyond lock-based programs, and demonstrate the applicability of sequential reasoning for a significantly more involved model: (i) we handle C11-like atomic access and fences of different modes (from which locks can be implemented); (ii) the model of [9, 10] treats lock/unlock as unknown functional calls, thus forbids optimizations across locks (since they are not performed by CompCert) in contrast to our model that allows optimizations across atomics; (iii) we validate load introduction which is unsound in CPM (in fact, we found out that distinguishing read-only and write permissions, as done in
[9, 10], does not suffice when write-read races are not UB, and developed the idea of written locations set (F) instead; and (iv) the target model in [9, 10] is x86-LSB, which is much simpler than the promising model studied here. All these aspects pose significant challenges in the design of the sequential model and its adequacy proof.

Certified compilation of concurrent programs. Jiang et al. [16] presented CASCompCert, an extension of CompCert deriving certified compilation of concurrent programs from the correctness of sequential compilation, which, in particular, preserves termination. The main difference from our work is that CASCompCert targets DRF programs under sequential consistency (SC), and assumes that racy code (e.g., for the implementation of locks) is confined in manually written assembly assuming x86-LSB and has race-free SC abstractions. As [9, 10], CASCompCert does not support optimizations across locked regions, reordering of non-atomic and atomic events, and load introduction.

Another extension of CompCert, called thread-safe CompCertX, was presented by Gu et al. [13] in the context of the certified concurrent abstraction layers framework (CCAL). They assume SC as the underlying model, and do not support optimizations on shared non-atomic, which are ubiquitous in concurrent programming.

Earlier work extended CompCert to concurrency [39, 42, 43], for the case that both the source and the target programs have x86-LSB semantics [31] using direct TSO reasoning for the relevant optimization passes. In our terms, this assumes that all accesses are atomic with semantics stronger than release/acquire, rendering various optimizations on non-racy code unsound. Indeed, these optimizations are not performed in the optimization passes of CompCertLSB.

Verification of compiler transformations. Many papers study the correctness of compiler optimizations under certain weak memory models. In particular, Burckhardt et al. [4] develop a denotational approach for compiler optimizations based on the rewritings performed by the target architecture; Ševčík [40] investigates optimizations under a general catch-fire model using locks and synchronization (a.k.a. volatile) accesses; and Vafeiadis et al. [38] provide an extensive study (in Coq) of program transformations in the C/C++11 model [2]. The approach of [38] requires understanding of the C/C++11 model and reasoning about all possible contexts. Another important difference is that the claims in [38] are on the trace-level (represented by execution graphs) leaving implicit the connection to programs.

Based on [38], testing methods and tools for checking the correctness of compiler optimizations were developed [5, 30] and applied on randomly generated programs. Roughly speaking, these validators match (full program) source and target executions and check that the matching adheres to the set of allowed transformations.

Dodds et al. [11] developed a technique and a tool for verifying transformations in the fragment of C11 consisting of release/acquire atoms, non-atomics, and SC-fences. They presented a denotational framework for establishing contextual refinement and provided a push-button tool (which does not support non-atomics) using the Alloy model checker.

Program-logics-based approaches. Recently, Gähler et al. [12] developed a separation logic (based on Iris [17]) for contextual refinement in a catch-fire model with SC atoms, allowing, in particular, optimizations involving both atoms and non-atomics. Their refinement preserves termination under fairness assumptions, and allows certain optimizations that modify the memory layout mappings. Interestingly, they considered sequential reasoning as a limitation of previous work, but, as we show, such reasoning does not have to identify atomic accesses with external function calls, and is, thus, capable of reasoning about a variety of optimizations.

Earlier work developed a rely-guarantee relational framework, which also provides means for establishing soundness of program transformations in the presence of assumptions about the environment [25, 26]. It assumes SC as the underlying model, and requires rely-guarantee reasoning for encoding, e.g., data-race-freedom, versus sequential reasoning that ensures refinement under any context as we present.

Compilation scheme correctness. A compilation correctness proof is not only about optimizations, and should also include the correctness of the “mapping schemes” to different architectures. In particular, the aforementioned works, including [9, 10, 16], include the correctness of mappings targeting the x86-LSB architecture. Additional proofs of the correctness of mapping schemes between more complex models appear in [29, 35]. For the promising semantics, mapping correctness was established in Coq [22] for multiple architectures (and the proof trivially generalizes to the extension with non-atomics) via IMM [36]. The latter provides an intermediate model between the programming language models and the various multicore architectures, which can be adapted to accommodate revised models on both sides.

Acknowledgments

We thank the anonymous PLDI reviewers for their helpful feedback. Chung-Kil Hur is the corresponding author. Minki Cho, Sung-Hwan Lee, Dongjae Lee, and Chung-Kil Hur were supported by Samsung Research Funding Center of Samsung Electronics under Project Number SRFC-IT2102-03. Ori Lahav was supported by the Israel Science Foundation (grant number 1566/18) and by the Alon Young Faculty Fellowship. This research was supported in part by the European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation programme (grant agreement no. 851811).
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