Faster than zChaff: Tuning SAT Heuristic for Bounded Model Checking

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Abstract

We have been using bounded model checking for formal hardware verification with GRASP and later with zchaff. However, in order to cope with very large hardware designs we try to exploit bounded model checking specific characteristics to enhance SAT algorithms for our problem.

We tuned the VSIDS (Variable State Independent Decaying Sum) decision heuristic embedded in zchaff [4] in order to make the DPLL SAT algorithm especially efficient for Bounded Model Checking (BMC) problems and to check the conclusions of [5]. From our experimental results on a real life benchmark, we conclude differently than [5]; however our tuning significantly increases SAT efficiency for BMC problems.

The use of SAT methods for hardware verification by symbolic model checking has been introduced in the framework of Bounded Model Checking [1] and, since then, has enjoyed several successes in the formal verification community [2].

Optimizations have already been implemented on top of CMU BMC [1] and GRASP [6] in order to tune SAT solvers for bounded model checking [5]. We reproduced the main optimization (*i.e.* static ordering) of [5] on the top of the zchaff SAT solver [4] and benchmarked it on an internal IBM benchmark from real life bounded model checking problems. We have great variance in the results; sometimes this heuristic behaves extremely good - more than one order of magnitude faster than regular zchaff - but sometimes extremely bad - several order of magnitudes slower. We then focused on tuning the VSIDS [4] decision heuristic on the top of zchaff and we obtained significantly better results than with original zchaff.

References

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